DECLARATION

I, Minoru UCHIDA, a national of Japan, c/o Musashi Works of Renesas Technology Corp. of 20-1, Josuihoncho 5-chome, Kodaira-shi, Tokyo, Japan, do hereby solemnly and sincerely declare:

1) THAT I am well acquainted with the Japanese language and English language, and
2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 1994-316444 filed on December 20, 1994.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 19 day of August, 2009.

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[Claims]

1. A semiconductor device comprising a base substrate, a semiconductor pellet mounted over a pellet mounting area of a main surface of the base substrate, external terminals arranged over a main surface of the semiconductor pellet, and first electrode pads arranged over a back surface of the base substrate and coupled electrically to the external terminals,

wherein the semiconductor pellet is mounted over the pellet mounting area of the main surface of the base substrate in a state in which the main surface of the semiconductor pellet faces down, second electrode pads coupled electrically to the first electrode pads are arranged over the back surface of the base substrate, and the external terminals of the semiconductor pellet and the second electrode pads of the base substrate are coupled together electrically with bonding wires through a slit formed in the base substrate.

2. A semiconductor device according to claim 1, wherein the slit is formed in a layout direction of the external terminals arranged plurally over the main surface of the semiconductor pellet and is arranged over the external terminals of the semiconductor pellet.

3. A semiconductor device according to claim 1 or claim 2,

wherein the second electrode pads of the base substrate are arranged respectively in both side areas of the back surface of the base substrate partitioned by the slit.

4. A semiconductor device according to claim 3, wherein electric power is applied to the second electrode pads arranged in one area of the back surface of the base substrate partitioned by the slit, while a signal is applied to each of the second electrode pads arranged in the other area of the back surface of the base substrate partitioned by the slit.

5. A semiconductor device according to any of claims 1 to 4, wherein the back surface of the semiconductor pellet is exposed from a sealing body which covers a peripheral area of the main surface of the base substrate from above.

6. A semiconductor device according to any of claims 1 to 5, wherein the bonding wires are sealed with a sealing body.

7. A semiconductor device according to any of claims 1 to 6, wherein bump electrodes are formed respectively over surfaces of the first electrode pads of the base substrate.

[Detailed Description of the Invention]

[0001]

[Industrial Application Field]

The present invention relates to a semiconductor device. Particularly, the present invention is concerned with a technique applicable effectively to a semiconductor device in which a semiconductor pellet is mounted on a pellet mounting area of a main surface of a base substrate, and external terminals arranged on a main surface of the semiconductor pellet and electrode pads arranged on a back surface of the base substrate are connected electrically.

[0002]

[Prior Art]

As a semiconductor device affording a high packaging density there is known a semiconductor device which adopts a BGA (Ball Grid Array) structure. In the semiconductor device adopting the BGA structure, as shown in Fig. 10 (a sectional view of a principal portion), a semiconductor pellet 2 is mounted on a pellet mounting area of a main surface of a base substrate 1 and plural bump electrodes 4 are arranged lattice-like on a back surface side opposite to the main surface of the base substrate 1.

[0003]

For example, the base substrate 1 is comprised of a printed

wiring substrate of a two-layer wiring structure. Plural electrode pads 1A are arranged in a peripheral area (around the pellet mounting area) of the main surface of the base substrate 1. Moreover, plural electrode pads 1B are arranged on the back surface opposite to the main surface of the base substrate 1. The electrode pads 1A are connected electrically to through-hole wiring lines 1C via wiring lines $1A_1$ arranged on the main surface of the base substrate 1. The electrode pads 1B are connected electrically to the through-hole wiring lines 1C via wiring lines $1B_1$ arranged on the back surface of the base substrate 1. Bump electrodes 4 are connected electrically and mechanically onto surfaces of the electrode pads 1B.

[0004]

The semiconductor pellet 2 is mainly comprised of a semiconductor substrate 2B which is formed of a single crystal silicon for example. A logic circuit system, a memory circuit system, or a mixed circuit system thereof, is mounted on a main surface (an elements-forming surface) of the semiconductor substrate 2B. Plural external terminals (bonding pads) 2A are also arranged on the main surface of the semiconductor substrate 2B. The external terminals 2A are formed in the top wiring layer out of wiring layers formed on the main surface of the semiconductor substrate 2B.

[0005]

The external terminals 2A of the semiconductor pellet 2 are connected electrically via bonding wires 6 to the electrode pads 1A arranged on the main surface of the base substrate 1. That is, the external terminals 2A of the semiconductor pellet 2 are connected electrically to the electrode pads 1B via bonding wires 3, electrode pads 1A, wiring lines $1A_1$, through-hole wiring lines 1C and wiring lines $1B_1$.

[0006]

The semiconductor pellet 2 and the bonding wires 6 are sealed with a sealing body 7 formed on the main surface of the base substrate 1.

[0007]

The semiconductor device thus configured is mounted onto a mounting surface of a mounting substrate and the bump electrodes 4 of the semiconductor device and the electrode pads arranged on the mounting surface of the mounting substrate are connected together electrically and mechanically.

[0008]

As to the semiconductor device adopting the foregoing BGA structure, it is described, for example, in NIKKEI ELECTRONICS published by Nikkei MacGraw-Hill, Inc. (February 28, 1994, pp. 111-117).

[0009]

[Problems to be Solved by the Invention]

In the above semiconductor device, the electrode pads 1A arranged on the main surface of the base substrate 1 are connected electrically via through-hole wiring lines 1C to the electrode pads 1B arranged on the back surface of the base substrate 1. Each through-hole wiring line 1C is comprised of a hole region formed within a through hole in the base substrate 1 and land regions (fringe portions) formed on both main surface and back surface of the base substrate 1. An inside diameter of the through hole is set at, for example, 0.3 mm and an outside diameter of each land region of the through-hole wiring line 1C is set at, for example, 0.6 mm. The inside diameter of the through hole and the outside diameter of each land region of the through-hole wiring line 1C are each set larger than the wiring width of each wiring line $1A_1$ (or $1B_1$) which provides an electrical connection between each electrode pad 1A (or 1B) and the associated through-hole wiring line 1C.

[0010]

On the other hand, the circuit system mounted on the semiconductor pellet 2 tends to become higher in the degree of integration, and with such a higher integration degree of the circuit system, the number of external terminals 1A of the semiconductor pellet 2 and that of the electrodes 1A of the base substrate 1A increase. That is, as the integration degree of the circuit system becomes higher, the number of through-hole

wiring lines 1C for electrical connection between the electrode pads 1A and 1B increases. Consequently, the outline size of the base substrate 1 becomes larger to a degree corresponding to the increase in the number of through-hole wiring lines 1C, thus giving rise to the problem that the size of the semiconductor device becomes larger.

[0011]

As the number of through-hole wiring lines 1C increases, the through-hole wiring lines 1C are arranged at distant positions from the semiconductor pellet 2 toward the outside. Consequently, the wiring lines $1A_1$ (or $1B_1$) which provide electrical connections between the electrode pads 1A (or 1B) and the through-hole wiring lines 1C become longer, thus giving rise to the problem that the inductance increases and the operating speed of the semiconductor device decreases.

[0012]

It is an object of the present invention to provide a technique capable of attaining the reduction in size of a semiconductor device.

[0013]

It is another object of the present invention to provide a technique capable of attaining a high operating speed of a semiconductor device.

[0014]

The above and other objects and novel features of the present invention will become apparent from the following description and the accompanying drawings.

[0015]

[Means for Solving the Problems]

The following is a brief description of a typical mode of the present invention as disclosed herein.

[0016]

A semiconductor device comprising a base substrate, a semiconductor pellet mounted over a pellet mounting area of a main surface of the base substrate, external terminals arranged over a main surface of the semiconductor pellet, and first electrode pads arranged over a back surface of the base substrate and coupled electrically to the external terminals, the semiconductor pellet being mounted over the pellet mounting area of the main surface of the base substrate in a state in which the main surface of the semiconductor pellet faces down, second electrode pads coupled electrically to the first electrode pads being arranged over the back surface of the base substrate, and the external terminals of the semiconductor pellet and the second electrode pads of the base substrate being coupled together electrically with bonding wires through a slit formed in the base substrate.

[0017]

[Operation]

According to the above means, since the external terminals of the semiconductor pellet and the first electrode pads of the base substrate can be coupled together electrically through bonding wires and second electrode pads, it is possible to omit through-hole wiring lines for electrical coupling between the electrode pads arranged on the main surface of the base substrate and the first electrode pads arranged on the back surface of the base substrate and the outline size of the base substrate can be reduced to a degree corresponding to the area (land region area) occupied by the through-hole wiring lines. As a result, it is possible to attain the reduction in size of the semiconductor device.

[0018]

Moreover, since the first electrode pads can be drawn nearer to the second electrode pads by a distance corresponding to the area occupied by the through-hole wiring lines, it is possible to shorten the wiring lines of the base substrate for electrical coupling between the second electrode pads and the first electrode pads. As a result, it is possible to decrease inductance and hence possible to attain a high operating speed of the semiconductor device.

[0019]

[Embodiments]

The construction of the present invention will be described hereinunder by way of embodiments thereof in which the present invention is applied to semiconductor devices each adopting a BGA structure.

[0020]

In all the drawings for illustrating the embodiments, portions having the same functions are identified by the same reference numerals, and repeated explanations thereof will be omitted.

[0021]

(First Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a first embodiment of the present invention is shown in Fig. 1 (a plan view on a main surface side), Fig. 2 (a sectional view taken on line A-A in Fig. 1), Fig. 3 (an enlarged sectional view of a principal portion in Fig. 2) and Fig. 4 (an enlarged plan view of a principal portion on a back side with a sealing body on the back side removed).

[0022]

In the semiconductor device of this first embodiment, as shown in Figs. 1, 2, 3 and 4, a semiconductor pellet 2 is mounted on a pellet mounting area of a main surface of a base substrate 1 and plural bump electrodes 4 are arranged lattice-like on a

back surface side opposite to the main surface of the base substrate 1.

[0023]

The base substrate 1 is, for example, a printed wiring substrate of a two-layer wiring structure. Plural electrode pads 1A and plural electrode pads 1B are arranged on the back surface of the base substrate 1. The electrode pads 1B and 1B are respectively connected with each other electrically through wiring lines $1B_1$ arranged on the back surface of the base substrate 1.

[0024]

The bump electrodes 4 are connected onto surfaces of the electrode pads 1B electrically and mechanically. For example, the bump electrodes 4 are formed of Pb-Sn alloy.

[0025]

The semiconductor pellet 2 is mounted on the pellet mounting area of the main surface of the base substrate 1 in a state in which a main surface (a lower surface in Figs. 2 and 3) of the semiconductor pellet faces down. That is, the semiconductor pellet 2 is mounted in a face-down manner onto the pellet mounting area of the main surface of the base substrate 1. An insulating layer 3 is interposed between the main surface of the semiconductor pellet 2 and the pellet mounting area of the main surface of the base substrate 1. For

example, the insulating layer 3 is formed of polyimide resin, epoxy resin, or silicon resin.

[0026]

For example, the semiconductor pellet 2 is formed in a rectangular shape in plan. The semiconductor pellet 2 is mainly comprised of a semiconductor substrate 2B which is formed of a single crystal silicon for example. A logic circuit system, a memory circuit system, or a mixed circuit system thereof, is mounted on a main surface (elements-forming surface) of the semiconductor substrate 2B. Moreover, on the main surface of the semiconductor substrate 2B, plural external terminals (bonding pads) 2A are arranged along each side of the rectangular shape. The external terminals 2A are formed in the top wiring layer out of wiring layers formed on the main surface of the semiconductor substrate 2B. That is, along the outer periphery of the main surface of the semiconductor pellet 2 there are arranged plural external terminals 2A for each side.

[0027]

The external terminals 2A on each side of the semiconductor pellet 2 and the associated electrode pads 1A on the base substrate 1 are connected together electrically with bonding wires 6 through a slit 5 formed in the base substrate 1. For example, the bonding wires 6 are each formed by gold (Au) wire, copper (Cu) wire, aluminum (Al) wire, or a coated

wire obtained by coating the surface of a metal wire with an insulating resin. The bonding wires 6 are bonded for example by a thermosonic wire bonding method.

[0028]

The slit 5 is formed in the arranged direction of the external terminals arranged plurally along one side of the main surface of the semiconductor pellet 2. The slit 5 is formed for each side of the semiconductor pellet 2. That is, four slits 5 are formed in the base substrate 1 used in this embodiment. The four slits 5 are formed on the external terminals 2A respectively on the four sides of the semiconductor pellet 2.

[0029]

The electrode pads 1A on the base substrate 1 are arranged in both side areas on the back surface of the base substrate 1 partitioned by the slits. Electric power, for example, an operating potential (e.g., 3.3 [V]) or a reference potential (e.g., 0 [V]), is applied to the electrode pads 1A arranged in one area (an inner area with respect to the semiconductor pellet 2) of the back surface of the base substrate 1 partitioned by the slits 5. On the other hand, a signal, e.g., an input/output signal or control signal, is applied to the electrode pads 1A arranged in the other area (an outer area with respect to the semiconductor pellet 2) of the back surface of the base substrate 1 partitioned by the slits.

[0030]

In the semiconductor pellet 2, for example one hundred external terminals 2A are arranged for each side of the semiconductor pellet 2 and layout pitch thereof is set at, for example, 100 [μm] or so. The number of external terminals 2A is increased with an increase in the degree of integration and in the operating speed of the circuit system mounted on the semiconductor pellet 2.

[0031]

In the base substrate 1, the electrode pads 1A arranged in one area of the back surface of the base substrate 1 partitioned by the slits 5 are arranged, for example, fifty for each side of the semiconductor pellet 2 and the electrode pads 1A arranged in the other area of the back surface of the base substrate 1 partitioned by the slits 5 are arranged, for example, fifty for each side of the semiconductor pellet 2. Since the electrode pads 1A cannot be microfabricated like the external terminals 2A of the semiconductor pellet 2, the layout pitch thereof is set wider than that of the external terminals 2A and, for example, it is set at 200 [μm] or so. That is, the electrode pads 1A of the base substrate 1 are arranged in two rows for each side of the semiconductor pellet 2, so even if the layout pitch of the electrode pads 1A on the base substrate 1 is set twice as wide as that of the external terminals 2A on the

semiconductor pellet 2, not only the layout length of the electrode pads 1A for each side of the semiconductor pellet 2 can be made almost equal to that of the external terminals 2A arranged on one side of the semiconductor pellet 2, but also the electrode pads 1A of the base substrate 1 can be arranged at positions opposed to the external terminals 2A of the semiconductor pellet 2.

[0032]

The peripheral area exclusive of the pellet mounting area of the main surface of the base substrate 1 is covered with a sealing body 7 from above and the bonding wires 6 are sealed with the sealing body 7. That is, the sealing body 7 is formed on both main surface and back surface of the base substrate 1. The sealing body 7 is formed, for example, by a transfer molding method. For the purpose of attaining a lower stress, the sealing body 7 is formed of an epoxy phenol curing resin incorporating silicone rubber and filler. The sealing body 7 may be formed by a potting method. Further, as shown in Fig. 5 (a sectional view), the sealing body 7 may be formed on the back surface of the base substrate 1 exclusive of the upper portions of the regions of the electrode pads 1A and 1B.

[0033]

A back surface opposite to the main surface of the semiconductor pellet 2 is exposed from the sealing body 7 which

covers the peripheral area of the base substrate 1.

[0034]

The semiconductor device thus configured is mounted onto a mounting surface of a mounting substrate and the bump electrodes 4 of the semiconductor device and electrode pads arranged on the mounting surface of the mounting substrate are connected together electrically and mechanically.

[0035]

Thus, the following functions and effects are obtained according to this first embodiment.

[0036]

(1) In the semiconductor device of the BGA structure wherein the semiconductor pellet 2 is mounted on the pellet mounting surface of the main surface of the base substrate 1 and the electrode pads (first electrode pads) 1B arranged on the back surface of the base substrate 1 are connected electrically to the external terminals 2A arranged on the main surface of the semiconductor pellet 2, the semiconductor pellet 2 is mounted on the pellet mounting area of the main surface of the base substrate 1 in a state in which the main surface of the semiconductor pellet 2 faces down, the electrode pads (second electrode pads) 1A connected electrically to the electrode pads 1B are arranged on the back surface of the base substrate 1 and the external terminals 2A of the semiconductor pellet 2 and the

electrode pads 1B of the base substrate 1 are connected together electrically with bonding wires 6 through the slits formed in the base substrate 1. According to this construction, the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1B of the base substrate 1 can be connected together electrically through the bonding wires 6 and the electrode pads 1A, so that it is possible to omit through-hole wiring lines (1C) which provide electrical connections between the electrode pads (1A) arranged on the main surface of the base substrate 1 and the electrode pads 1B arranged on the back surface of the base substrate. Moreover, the outline size of the base substrate 1 can be reduced to a degree corresponding to the area (land region area) occupied by the through-hole wiring lines. As a result, it is possible to attain the reduction in size of the semiconductor device.

[0037]

Further, since the electrode pads 1B can be drawn closer to the electrode pads 1A by a distance corresponding to the area occupied by the through-hole wiring lines, it is possible to shorten the wiring liens $1B_1$ of the base substrate 1 which lines provide electrical connections between the electrode pads 1A and 1B. As a result, it is possible to shorten the signal paths between the electrode pads 1A and 1B and hence possible to diminish inductance, thus making it possible to attain a high

operating speed of the semiconductor device.

[0038]

(2) The slits are formed in the layout direction of the plural external terminals 2A arranged on the main surface of the semiconductor pellet 2 and are arranged over the external terminals 2A of the semiconductor pellet 2. According to this construction, since the slits 5 are arranged within the area occupied by the semiconductor pellet 2, it is possible to suppress an increase in outline size of the base substrate 1 corresponding to the area occupied by the slits 5.

[0039]

(3) The electrode pads 1A are arranged in both side areas of the back surface of the base substrate 1 partitioned by the slits 5. According to this construction it is possible to increase the power supply paths which provide electrical connections between the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1. Consequently, it is possible to reduce power noise generated at the time of simultaneous switching of signals and hence possible to prevent a malfunction of the semiconductor device.

[0040]

Moreover, even if the layout pitch of the electrode pads 1A of the base substrate 1 is set wider than that of the external terminals 2A of the semiconductor pellet 2, the pad layout

length of the electrode pads 1A for each side of the semiconductor pellet 2 can be made almost equal to that of the external terminals 2A arranged on each side of the semiconductor pellet 2. Consequently, it is possible to prevent an increase in length of the bonding wires 6 attributable to the pad layout length of the electrode pads 1A and, at the time of sealing the bonding wires 6 with the sealing body 7 in accordance with the transfer molding method, it is possible to prevent wire deformation of the bonding wires 6 caused by flowing of resin.

[0041]

Further, since the electrode pads 1A of the base substrate 1 can be arranged at the position opposed to the external terminals 2A of the semiconductor pellet 2, the bonding wires 6 can be made uniform in length and hence it is possible to make uniform the inductance of the signal paths between the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1.

[0042]

(4) The back surface opposed to the main surface of the semiconductor pellet 2 is exposed from the sealing body 7 which covers the peripheral area of the main surface of the base substrate 1 from above. According to this construction, the heat generated with operation of the circuit system mounted on the semiconductor pellet 2 can be released to the exterior from

the back surface of the semiconductor pellet 2, so that it is possible to enhance the heat dissipating efficiency of the semiconductor device.

[0043]

(5) The bonding wires 6 are sealed with the sealing body 7. According to this construction, it is possible to prevent deformation of the bonding wires 6 caused by external shock or contact and hence possible to enhance the electrical reliability of the semiconductor device.

[0044]

(6) The sealing body 7 is formed on both main surface and back surface of the base substrate 1. According to this construction, it is possible to prevent the sealing body 7 from being peeled from the base substrate 1 due to a thermal stress generated in a temperature cycle test or at the time of connection of the bump electrodes 4 and hence possible to enhance the reliability of the semiconductor device.

[0045]

(Second Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a second embodiment of the present invention is shown in Fig. 6 (a sectional view) and Fig. 7 (an enlarged plan view of a principal portion on a back surface side with a sealing body on the back surface side

removed).

[0046]

In the semiconductor device of this second embodiment, as shown in Figs. 6 and 7, a semiconductor pellet 2 is arranged on a pellet mounting area of a main surface of a base substrate 1 through an insulating layer 3 by a face-down method and plural bump electrodes 4 are arranged lattice-like on a back surface side of the base substrate 1.

[0047]

Plural external terminals 2A are arranged at a center of a main surface of the semiconductor pellet 2 and along long sides of the main surface. The external terminals 2A are connected respectively to plural electrode pads 1A electrically with bonding wires 6 through a slit 5 formed in the base substrate 1, the electrode pads 1A being formed on the back surface of the base substrate 1. The electrode pads 1A are connected respectively to plural electrode pads 1B electrically through wiring lines $1B_1$, the electrode pads 1B being formed on the back surface of the base substrate 1. The bump electrodes 4 are connected respectively onto the surfaces of the electrode pads 1B electrically and mechanically. That is, the external terminals 2A of the semiconductor pellet 2 are connected to the electrode pads 1B electrically through bonding wires 6, electrode pads 1A and wiring lines $1B_1$.

[0048]

The slit 5 of the base substrate 1 is formed in the layout direction of the external terminals 2A which are arranged at a center of the main surface of the semiconductor pellet 2 and along long sides of the main surface. The slit 5 is formed in a tapered shape having an aperture size on the main surface side of the base substrate 1 smaller than that on the back surface side of the base substrate.

[0049]

Thus, according to this second embodiment, not only the same functions and effects as in the previous first embodiment are obtained, but also, by forming the slit 5 in a tapered shape, it is possible to prevent contact between the base substrate 1 and a bonding tool when bonding one ends of the bonding wires 6 to the external terminals 2A on the semiconductor pellet 2, so that it is possible to enhance the semiconductor device assembling yield in the bonding process.

[0050]

(Third Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a third embodiment of the present invention is shown in Fig. 8 (a plan view of a principal portion on a back surface side with a sealing body on the back surface side removed).

[0051]

In the semiconductor device of this third embodiment, as shown in Fig. 8, a semiconductor pellet 2 is mounted onto a pellet mounting area of a main surface of a base substrate 1 through an insulating layer (3) by a face-down method and plural bump electrodes 4 are arranged lattice-like on a back surface side of the base substrate 1.

[0052]

Plural external terminals 2A are arranged on the outer periphery of a main surface of the semiconductor pellet 2 and along four sides of the main surface. Further, at the center of the main surface of the semiconductor pellet 2 there are arranged plural external terminals 2A along long or short sides of the main surface. The external terminals 2A are coupled respectively to plural electrode pads 1A electrically with bonding wires 6 through slits 5 formed in the base substrate 1, the electrode pads 1A being arranged on the back surface of the base substrate 1. The electrode pads 1A are connected respectively to plural electrode pads 1B electrically through wiring lines ($1B_1$), the electrode pads 1B being arranged on the back surface of the base substrate 1. Bump electrodes 4 are connected respectively onto the surfaces of the electrode pads 1B electrically and mechanically. That is, the external terminals 2A of the semiconductor pellet 2 are connected to the

electrode pads 1B electrically through bonding wires 6, electrode pads 1A and wiring lines $1B_1$.

[0053]

The slits 5 of the base substrate 1 are positioned not only on each side but also at the center of the semiconductor pellet 2. That is, in this third embodiment, five slits 5 are formed in the base substrate 1. The five slits 5 are arranged over the external terminals 2A of the semiconductor pellet 2.

[0054]

Thus, according to this third embodiment there are obtained the same functions and effects as in the foregoing first embodiment. Besides, by arranging the slits 5 on each side of the semiconductor pellet 2 and also at the center of the semiconductor pellet, not only it is possible to increase the number of electrode pads 1A arranged on the back surface of the base substrate 1, but also it is possible to increase the power supply paths which provide electrical connections between the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1. Consequently, it is possible to further reduce power noise generated at the time of simultaneous switching of output signals. Moreover, it is possible to increase the signal paths which provide electrical connections between the external terminals 2A of the semiconductor pellet 2 and the electrode

pads 1A of the base substrate 1 and hence possible to reduce the outline size of the semiconductor pellet 2 which restricted by the number of external terminals 2A.

[0055]

Although according to the construction of this third embodiment there is arranged one slit 5 at a center of the semiconductor pellet 2, plural slits 5 may be formed at the center of the semiconductor pellet 2 so as to be parallel or intersect each other, thus increasing the number of slits 5, whereby the number of electrode pads 1A of the base substrate 1 and that of the external terminals 2A of the semiconductor pellet 2 can be further increased.

[0056]

(Fourth Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a fourth embodiment of the present invention is shown in Fig. 9 (a plan view of a principal portion on a back surface side with a sealing body on the back surface side removed).

[0057]

In the semiconductor device of this fourth embodiment, as shown in Fig. 9, a semiconductor pellet 2 is mounted onto a pellet mounting area of a main surface of a base substrate 1 through an insulating layer (3) by a face-down method and

plural bump electrodes 4 are arranged lattice-like on a back surface side of the base substrate 1. For example, the base substrate 1 is a printed wiring substrate of a three-layer wiring structure.

[0058]

On the outer periphery of a main surface of the semiconductor pellet 2 there are arranged plural external terminals 2A along each side of the main surface. The external terminals 2A are connected respectively to plural electrode pads 1A electrically with bonding wires 6 through slits formed in the base substrate 1, the electrode pads 1A being arranged on the back surface of the base substrate 1.

[0059]

Of the electrode pads 1A, electrode pads $1A_2$ are formed integrally with electrode plates 8A. One electrode pad 8A is connected electrically to another electrode plate 8A through a through-hole wiring line (not shown) and an internal wiring line (not shown) of the base substrate 1. A reference potential (e.g., 0 [V]) is applied as electric power to each electrode plate 8A. Of the electrode pads 1A, electrode pads $1A_3$ are formed integrally with an electrode plate 8B. For example, an operating potential (e.g., 3.3 [V]) is applied as electric power to the electrode plate 8A.

[0060]

Thus, according to this fourth embodiment, through-hole wiring lines (1C) for electrical connection between the electrode pads (1A) arranged on the main surface of the base substrate 1 and the electrode pads 1B arranged on the back surface of the main surface are omitted, whereby the electrode plates 8A and 8B can be arranged on the back surface side of the base substrate 1. Consequently, the layout of the bump electrodes 4 can be set freely and it is possible to shorten the distance between the external terminals 2A of the semiconductor pellet 2 and the bump electrodes 4. As a result, it is possible to decrease inductance and hence possible to attain a high operating speed of the semiconductor device.

[0061]

Although the present invention has been described above concretely by way of the above embodiments, it goes without saying that the invention is not limited to the above embodiments, but that various changes may be made within the scope not departing from the gist of the invention.

[0062]

For example, the present invention is applicable to a semiconductor device having a base substrate 3 of a three- or more layer structure.

[0063]

[Effect of the Invention]

The following is a brief description of effects obtained by typical modes of the present invention as disclosed herein.

[0064]

It is possible to reduce the size of a semiconductor device wherein a semiconductor pellet is mounted on a pellet mounting surface of a main surface of a base substrate and electrode pads arranged on a back surface of the base substrate are connected electrically to external terminals arranged on a main surface of the semiconductor pellet.

[0065]

Further, it is possible to attain a high operating speed of the semiconductor device.

[Brief Description of the Drawings]

Fig. 1 is a plan view of a main surface side of a semiconductor device adopting a BGA structure according to a first embodiment of the present invention.

Fig. 2 is a sectional view taken on line A-A in Fig. 1.

Fig. 3 is an enlarged sectional view of a principal portion in Fig. 2.

Fig. 4 is an enlarged plan view of a principal portion on a back surface side of the semiconductor device with a sealing body on the back surface side removed.

Fig. 5 is a sectional view showing a modification of the semiconductor device.

Fig. 6 is a sectional view of a semiconductor device adopting a BGA structure according to a second embodiment of the present invention.

Fig. 7 is an enlarged plan view of a principal portion of a back surface side of the semiconductor device with a sealing body on the back surface side removed.

Fig. 8 is a plan view of a principal portion of a back surface side of a semiconductor device adopting a BGA structure according to a third embodiment of the present invention, with a sealing body on the back surface side removed.

Fig. 9 is a plan view of a principal portion of a back surface side of a semiconductor device adopting a BGA structure according to a fourth embodiment of the present invention, with a sealing body on the back surface side removed.

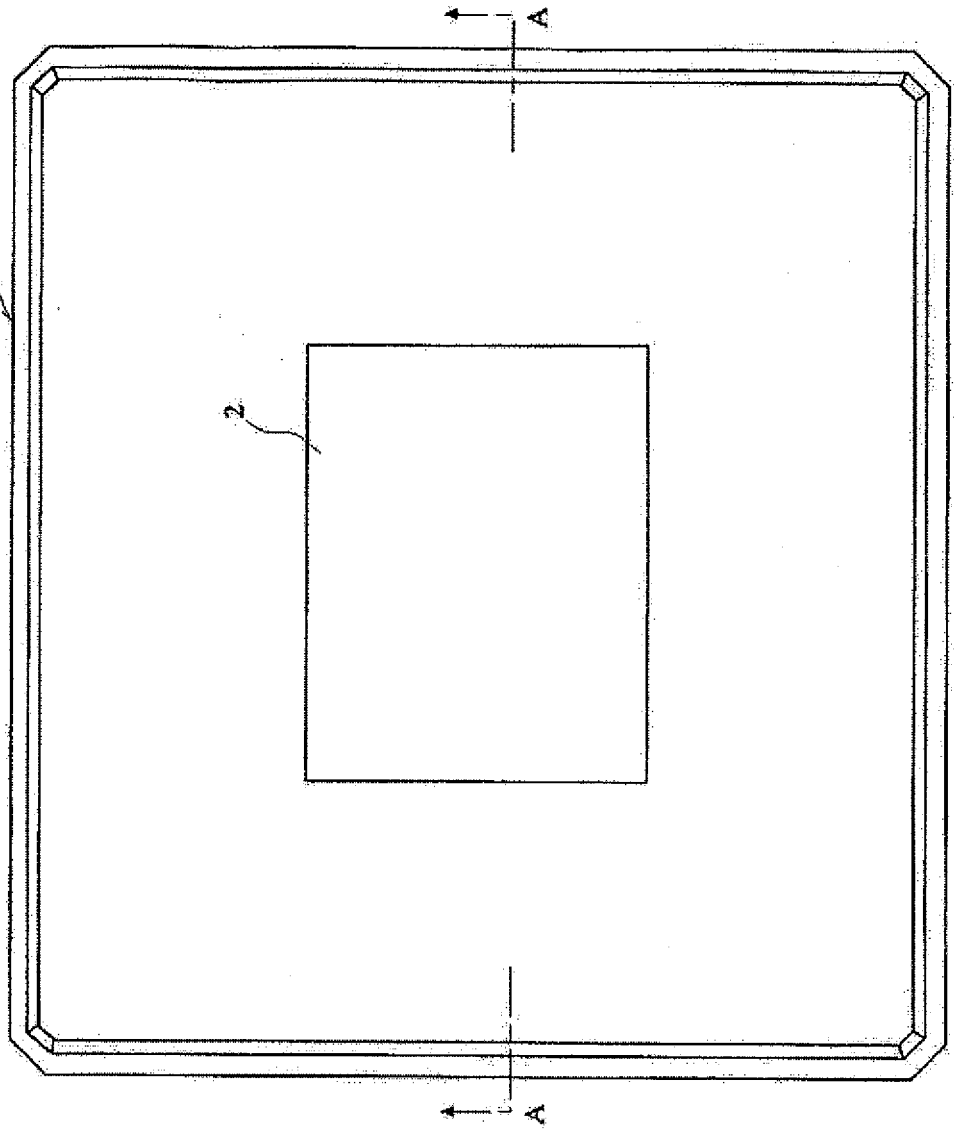
Fig. 10 is a sectional view of a principal portion of a conventional semiconductor device adopting a BGA structure.

[Explanation of Reference Numerals]

1 ... base substrate, 1A ... electrode pad, 1B ... electrode pad, 2 ... semiconductor pellet, 2A ... external terminal, 3 ... insulating layer, 4 ... bump electrode, 5 ... slit, 6 ... bonding wires, 7 ... sealing body, 8A, 8B ... electrode plate

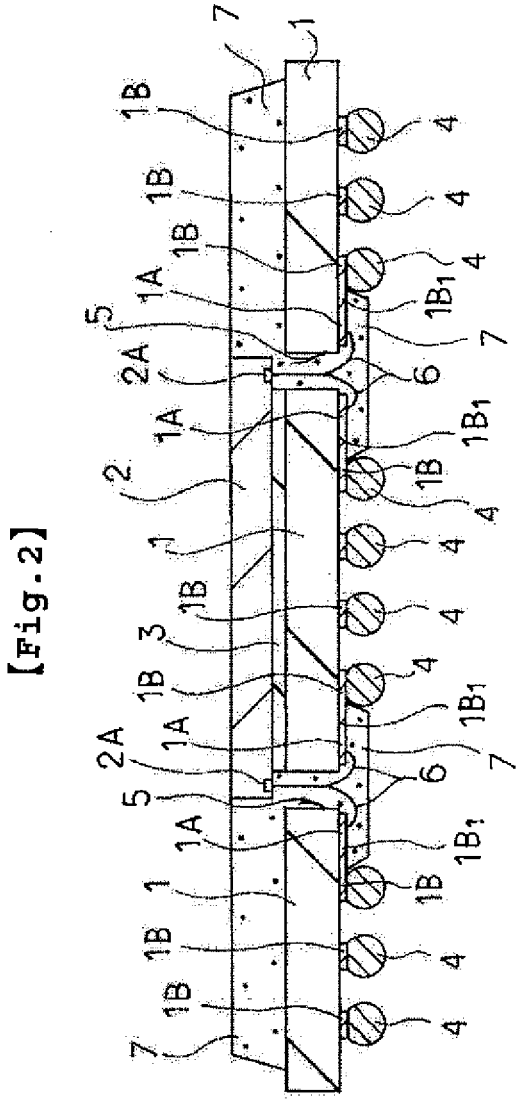
【Name of Document】 Drawing

【Fig.1】

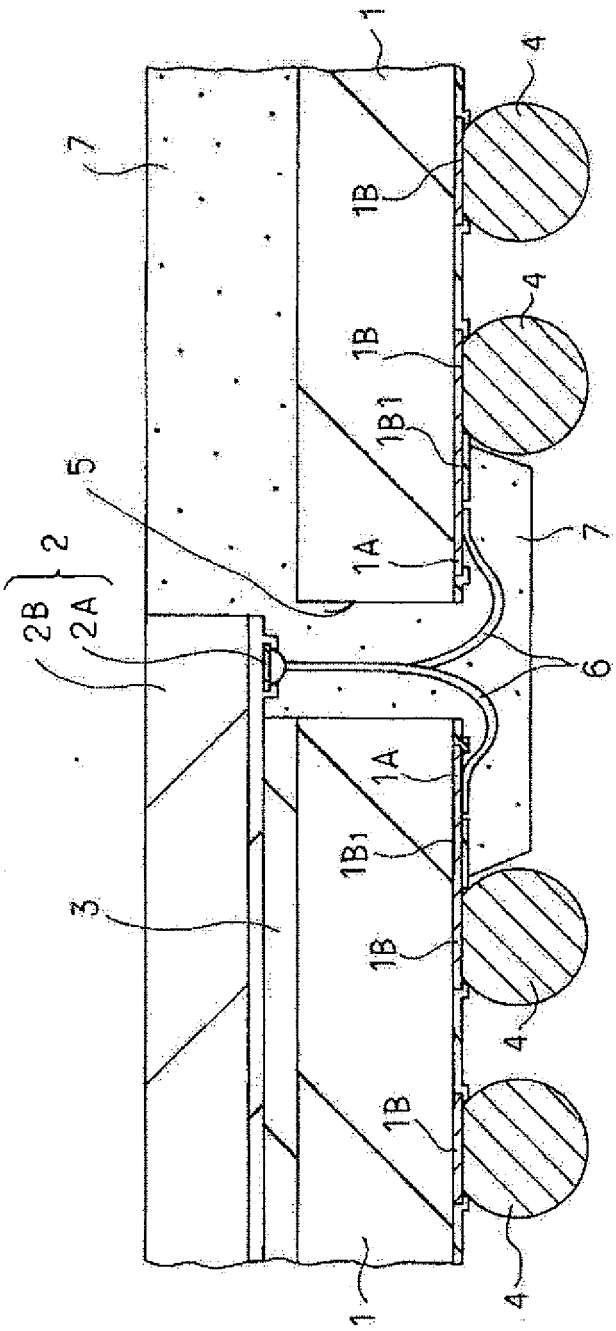


【Fig.1】

【Fig.2】

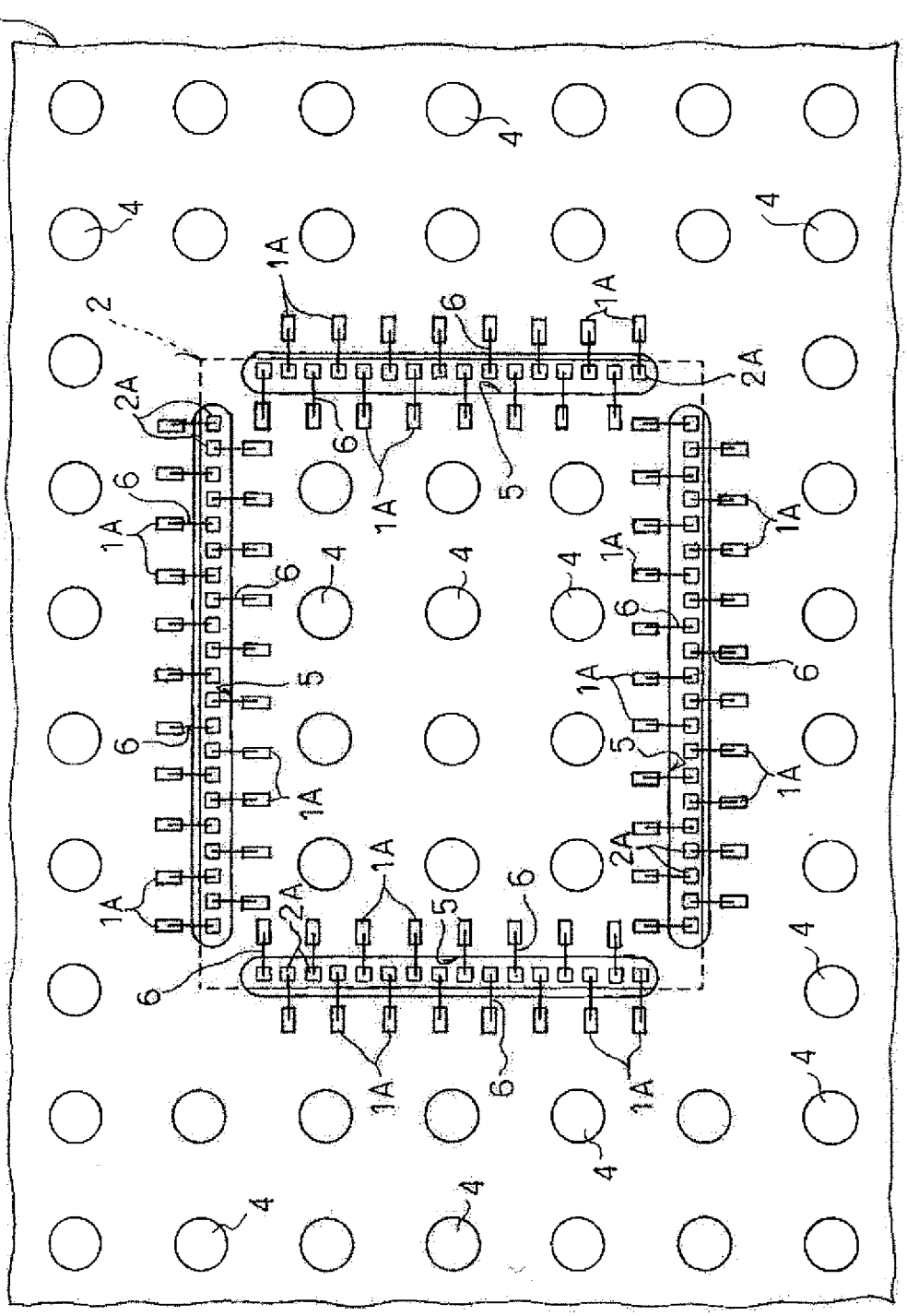


【Fig.3】



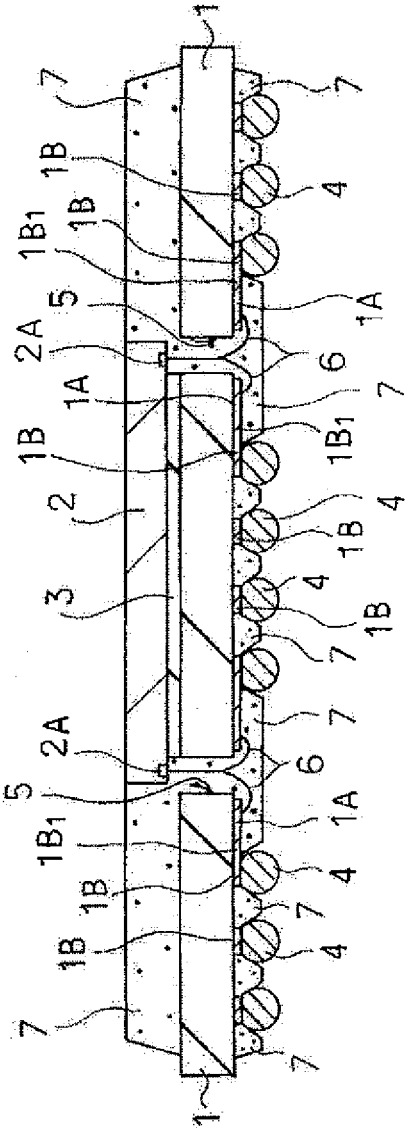
【Fig.3】

【Fig.4】



【Fig.4】

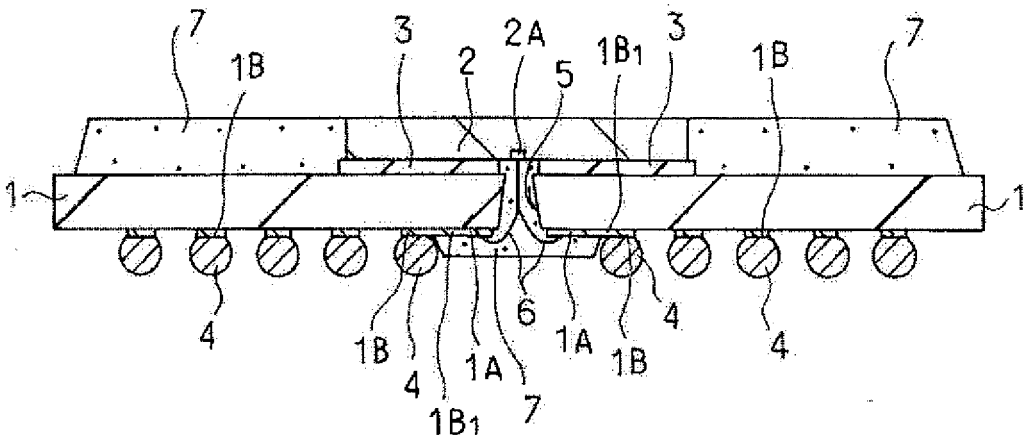
【Fig.5】



【Fig.5】

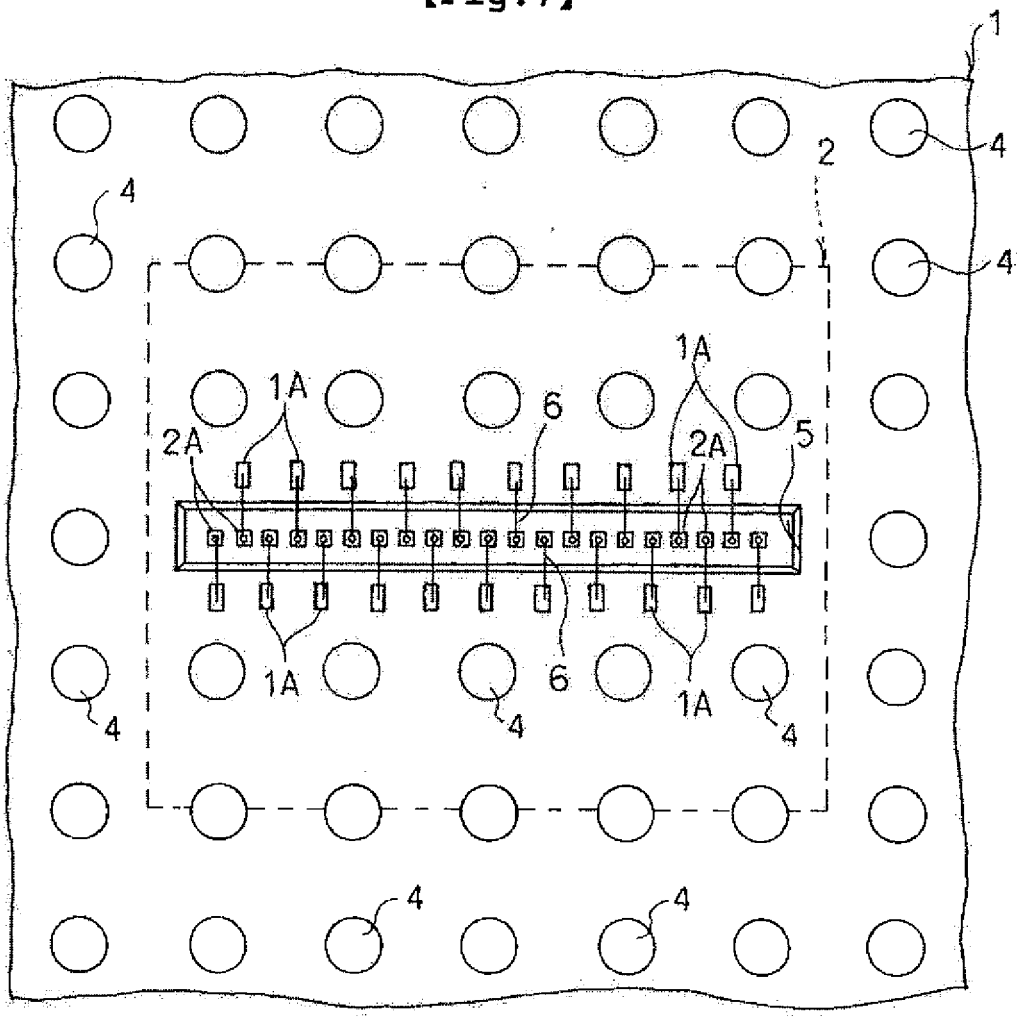
【Fig.6】

【Fig.6】

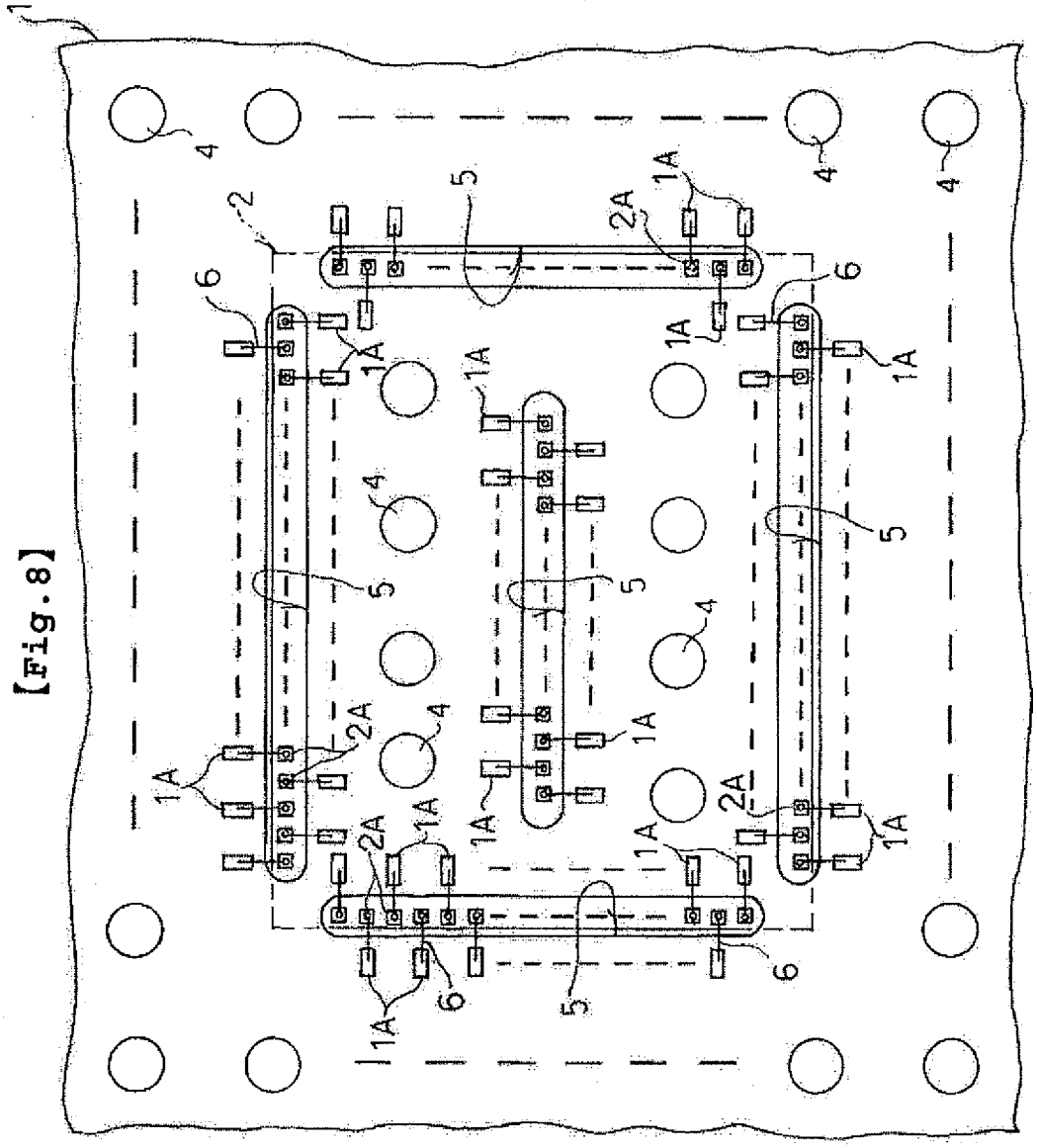


【Fig.7】

【Fig.7】

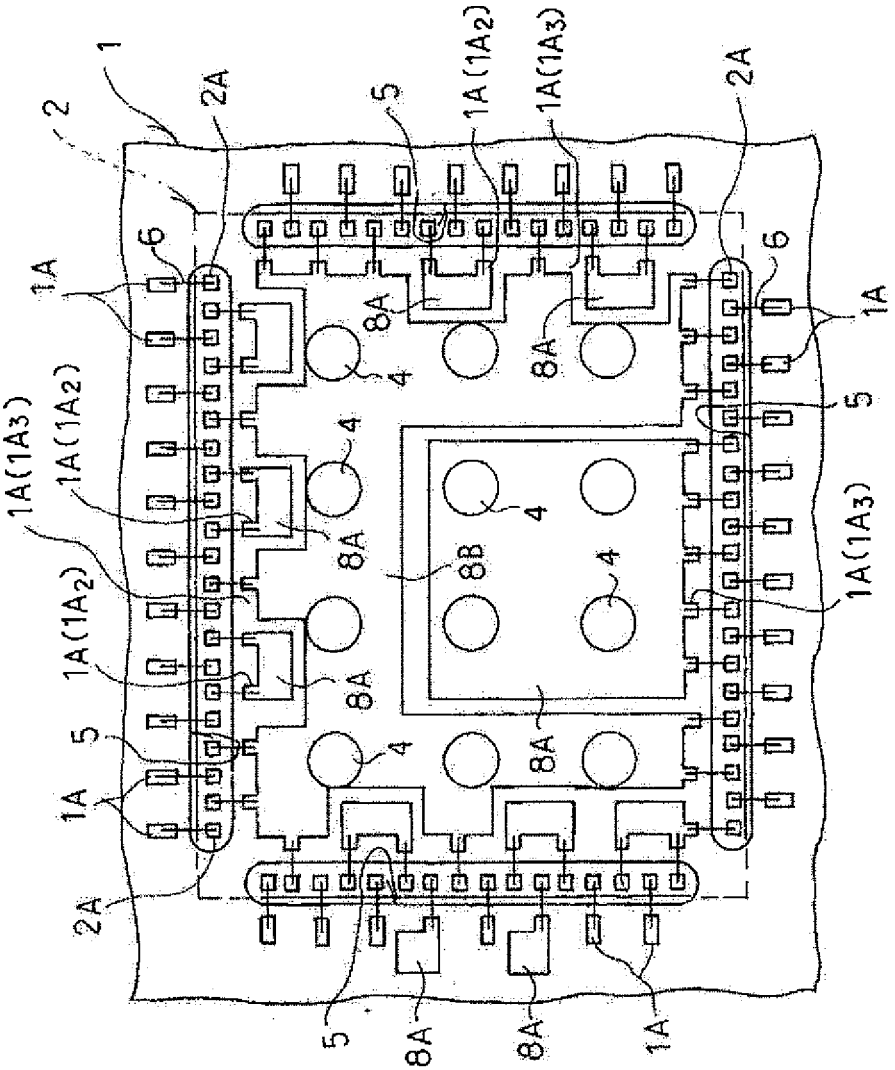


【Fig.8】



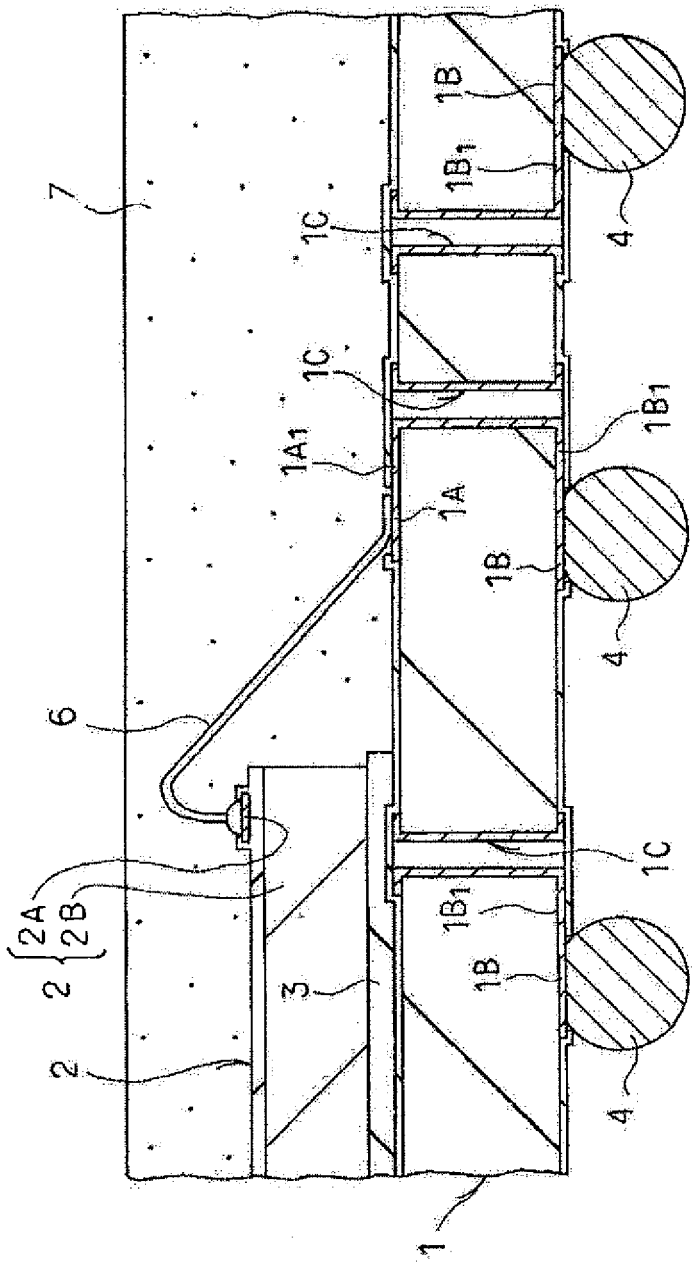
【Fig.8】

【Fig.9】



【Fig.9】

【Fig.10】



【Fig.10】

[Name of Document] Abstract

[Abstract]

[Object]

The size of a semiconductor device is to be reduced and a high operating speed of the semiconductor device is to be attained.

[Construction]

A semiconductor device comprising a base substrate 1, a semiconductor pellet 2 mounted on a pellet mounting area of a main surface of the base substrate 1, external terminals 2A arranged over a main surface of the semiconductor pellet 2, and first electrode pads 1B arranged over a back surface of the base substrate 1 and coupled electrically to the external terminals 2A, the semiconductor pellet 2 being mounted on the pellet mounting area of the main surface of the base substrate 1 in a state in which the main surface of the semiconductor pellet 2 faces down, second electrode pads coupled electrically to the first electrode pads being arranged over the back surface of the base substrate 1, and the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1 being coupled together electrically with bonding wires through a slit 5 formed in the base substrate 1.

[Selected Drawing] Fig. 3